IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Stefan Eder **GROUP:** 2838

INTERNATIONAL APPLN. NO.: PCT/DE00/01737 **EXAMINER:** Bao Q. Vu

SERIAL NO: 10/089,425

INTERNATIONAL FILING DATE: 29 May 2000

FOR: CIRCUIT COMPRISING AN INTEGRATED SWITCHING CIRCUIT AND A VOLTAGE REGULATING CIRCUIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

TRANSMITTAL LETTER

Enclosed herewith are three copies of the appellant's appeal brief.

Respectfully submitted,

Patrick O'Shea

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I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited on Monday, August 16, 2004 in an envelope with sufficient postage for first class mail addressed to the: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Patrick O'Shea

Patrick J. O'Shea

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Sir:

APPEAL BRIEF

This appeal is in response to the Official Action dated February 12, 2004, which has been made final. A check in the amount of $330 is enclosed herewith pursuant to 37 C.F.R. §1.17(c).

TABLE OF CONTENTS

I. REAL PARTY OF INTEREST

The real party of interest is Micronas GmbH of Freiburg, Germany, which is the successor by merger of Micronas Munich GmbH.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

On June 14, 2004 the appellant appealed from the final rejection of claims 1-3 and 8-12 under 35 U.S.C. §102(b). Claims 5-7 have been allowed. Claims 1-12, which are set forth in Appendix A attached hereto, are all the remaining claims in this application.

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF THE INVENTION

This invention relates to the field of integrated circuits, and in particular to an integrated circuit that includes an integrated switching circuit and a voltage regulating circuit, which furnishes a regulated voltage for the operation of the circuit.

VI. ISSUES

Whether claims 1-3 and 8-12 are anticipated by U.S. Patent 5,216,351 to Shimoda (hereinafter "Shimoda").

VII. GROUPING OF THE CLAIMS

Appellant believes that claims 1-3 stand and fall together, and that claims 8-12 stand and fall together.

VIII. ARGUMENT

CLAIM 1

Claim 1 recites a *"[c]ircuit comprising an integrated switching circuit (1) integrated on a substrate material, characterized in that a voltage regulating circuit (2) for the provision of a supply voltage (VG) is also integrated on the substrate material."* (emphasis added, cl. 1). Significantly, the circuit comprises (i) an integrated switching circuit and (ii) a voltage regulating circuit, both of which are integrated on the substrate material.

Shimoda simply discloses a voltage regulator that includes a switching regulator block 11 and a succeeding series regulator block 10, which are integrated onto one chip (see col. 2, lines 1-6). That is, in Shimoda the switching regulator block 11 and the succeeding series regulator block 10 combine to establish the voltage regulator (see col. 2, lines 1-6). The regulator blocks 10, 11 of Shimoda cooperate to provide a *"constantly regulated output voltage V_{OUT}."* (col. 2, lines 28-29). In contrast, the circuit recited in claim 1 includes a voltage regulator circuit **AND** a switching circuit. As recited in claim 1, the voltage regulator circuit *provides the regulated voltage* to the switching circuit. Shimoda merely discloses that regulator blocks 10, 11 disclosed

therein cooperate to form a voltage regulator that provides a regulated output voltage V_{OUT} – Shimoda neither discloses nor suggests a voltage regulator in combination with a switching circuit as recited in claim 1. There is no structure disclosed in Shimoda other than the structure employed to establish the voltage regulator, so there is no remaining structure in Shimoda that the integrated switching circuit recited in claim 1 can read on.

In response to the Applicant's contention in the Request for Reconsideration filed March 3, 2004, the Advisory Action dated March 30, 2004 states *"...one of ordinary skill in the art would know that a voltage regulator is the most common type of circui[t], in essence it is any type of circuit that regulates voltage. One of ordinary skill in the art would view both circuits as described in the prior art as both voltage regulator circuits as well as switching regulators."* However, these contentions are inconsistent with the unambiguous teaching of Shimoda, which clearly states *"FIG. 1 shows a block diagram of a voltage regulator according to the invention. The voltage regulator is comprised of a preceding switching regulator block 11 and a succeeding series regulator block 10, which are preferably integrated into one chip of a semiconductor device to form a monolithic MOS IC device."* (emphasis added, col. 2, lines 1-6). Shimoda teaches that a voltage regulator is established by combining blocks 10 and 11, while the Advisory Action contends, without citing to any portion of Shimoda, that a person of ordinary skill would view either block 10 or block 11 individually as a voltage regulator. However, this contention in the Advisory Action is wholly inconsistent with the unambiguous teaching of Shimoda that a voltage regulator is established by combining blocks 10 and 11. In addition, the statements in the Advisory Action fail to specify at what time in time a person of ordinary skill in the art would have taken the view suggested in the Advisory Action.

CLAIM 8

Claim 8 is patentable for at least the same reasons as set forth above. In addition, claim 8 recites that a voltage regulating circuit provides a *regulated* voltage signal **to a** switching circuit. However, in Shimoda, the switching regulator 11 provides an intermediate voltage signal *Vsw* **to the** series regulator block 10 (see FIG. 1), and the series regulator block 10 alone can not be read as a voltage regulator since Shimoda teaches that blocks 10 and 11 must be combined to form the voltage regulator. Accordingly, the structure of Shimoda is clearly incapable of anticipating the subject matter of claim 8.

SUMMARY OF DIFFERENCES

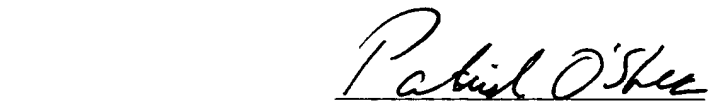
A 35 U.S.C. §102 rejection requires that a single reference teach ***each and every*** element of the claimed invention. Again, Shimoda neither discloses nor suggests a voltage regulator in combination with a switching circuit as recited in claims 1 and 8. Shimoda discloses only that blocks 10 and 11 combine to provide a voltage regulator. There is no structure in Shimoda other than blocks 10 and 11, so there is no structure that the claimed switching regulator can read on once the voltage regulator recited in the claims is read onto blocks 10 and 11 of Shimoda. In addition, Shimoda also fails to disclose a voltage regulating circuit that provides a regulated voltage signal to a switching regulator as recited in claim 8. Hence, Shimoda is incapable of anticipating the claimed invention.

CONCLUSION

For all the foregoing reasons, we submit that the rejection of claims 1-3 and 8-12 is erroneous and reversal thereof is respectfully requested.

If there are any fees due in connection with the filing of this appeal brief, please charge them to our Deposit Account 19-0079. If a fee is required for any extension of time under 37 C.F.R. §1.136 not accounted for above, such an extension is requested and the fee should be charged to the above Deposit Account.

Respectfully submitted,



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CLAIMS

1.(Original) Circuit comprising an integrated switching circuit (1) integrated on a substrate material, characterized in that a voltage regulating circuit (2) for the provision of a supply voltage (VG) is also integrated on the substrate material.

2.(Previously Presented) The circuit of claim 1, comprising an internal connection (5) in the circuit for feeding the supply voltage (VG) from the voltage regulating circuit (2) to the switching circuit (1).

3.(Previously Presented) The circuit of claim 2, comprising a contact (6) accessible outside the circuit, at which the supply voltage (VG) can be taken off.

4.(Previously Presented) Circuit comprising an integrated switching circuit (1) integrated on a substrate material, characterized in that a voltage regulating circuit (2) for the provision of a supply voltage (VG) is also integrated on the substrate material, characterized in that, on the substrate material, the switching circuit (1) is electrically isolated from the voltage regulating circuit (2) and the voltage regulating circuit (2) exhibits a contact (6) accessible outside the circuit, at which the supply voltage (VG) can be taken off.

5.(Previously Presented) The circuit of claim 4, wherein the contact (6) is connected to the switching circuit (1) via an electrical connection (9) led outside the substrate material.

6.(Previously Presented) The circuit of claim 5, wherein the contact (6) is connected to the switching circuit (1) via a switch (11).

7.(Previously Presented) Circuit according to one of Claims 1 to 6, characterized in that the switching circuit (1) is designed for telecommunications purposes and is controllable via a data bus (3).

8.(Previously Presented) An integrated circuit that receives a voltage signal, comprising:

a voltage regulating circuit that receives the voltage signal and provides a regulated voltage signal; and

a switching circuit that receives said regulated voltage signal to power said switching circuit.

9.(Previously Presented) The integrated circuit of claim 8, wherein said integrated circuit comprises an internal connection that provides said regulated voltage signal from said voltage regulating circuit to said switching circuit.

10.(Previously Presented) The integrated circuit of claim 8, wherein said integrated circuit comprises an external connection accessible at the exterior of said integrated circuit, and said regulated voltage signal is provided from said voltage regulating circuit along said external connection to said switching circuit.

11.(Previously Presented) The integrated circuit of claim 10, comprising an electrical insulator configured and arranged to electrically insulate said voltage regulating circuit from said switching circuit.

12.(Previously Presented) The integrated circuit of claim 9, comprising an external contact on said integrated circuit on which said voltage regulating circuit provides said regulated voltage signal.